IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A signal processing apparatus, comprising:

a second-order Volterra filter configured to equalize an input signal, wherein,

a quadratic section of said second-order Volterra filter configured to implement a quadratic term of said second-order Volterra filter includes a plurality of multiplication [[unit]] units configured to multiply a first input signal with a second input signal to produce a product signal, one of said plurality of multiplication units being configured to employ a signal not delayed from said first input signal, as said second input signal, a remaining one of said plurality of multiplication units being configured to employ a signal delayed a preset time from said first input signal, as said second input signal,

the one of said plurality of multiplication [[unit]] units including,

one or more delay units connected in series with one another and configured to delay a signal output from the one of said plurality of multiplication [[unit]] units, each by a unit time,

a multiplier configured to multiply [[a]] the signal output from the one of said plurality of multiplication [[unit]] units and a signal output from each of said one or more delay units, each with a preset coefficient, ~~said multiplier being further configured to update each preset coefficient every unit time,~~ and

an adder configured to sum outputs of said multiplier together,

wherein a step gain parameter for updating each preset coefficient of a multiplier of the remaining one of said plurality of multiplication units is twice a step gain parameter for updating each preset coefficient of the multiplier of the one of said plurality of multiplication units.

2. (Canceled)

3. (Currently Amended) The signal processing apparatus according to claim 1, wherein said ~~quadratic section~~ plurality of multiplication units includes n of said multiplication units, n being an integer not less than 1, a kth one of said plurality of multiplication units, k being an integer such that $1 \leq k \leq n$, being configured to employ a signal corresponding to said first input signal delayed by (k−1) times of said unit time as said second input signal.

4. (Currently Amended) A signal processing method, employing a second-order Volterra filter, for equalizing an input signal, the signal processing method comprising:

performing a processing equivalent to a quadratic term of said second-order Volterra filter including,

multiplying a first signal with a ~~second~~ signal not delayed from said first signal to produce a first product signal;

multiplying the first signal with a signal delayed a preset time from said first signal to produce a second product signal;

delaying the first product signal, by one or more series-connected delay units, each by a unit time;

multiplying the first product signal and a signal output from each of said one or more series-connected delay units, each with a preset coefficient to produce a plurality of addend signals,

multiplying the second product signal with a preset coefficient to produce an addend signal,

~~updating each preset coefficient every unit time,~~ and

summing the addend signal and the plurality of addend signals together, wherein a step gain parameter for updating the preset coefficient for multiplying the second product signal is twice a step gain parameter for updating each preset coefficient for multiplying the first product signal and the signal output from each of said one or more series-connected delay units.

5. (Currently Amended) A signal decoding apparatus, employing a second-order Volterra filter, for equalizing and decoding an input signal, the signal decoding apparatus comprising:

a linear section of the second-order Volterra filter, the linear section being configured to implement a linear term of said second-order Volterra filter and to linearly equalize said input signal;

a quadratic section of the second-order Volterra filter, the quadratic section being configured to implement a quadratic term of said second-order Volterra filter and to non-linearly equalize said input signal;

a first adder configured to sum a signal output from said linear section and a signal output from said quadratic section together; and

a processor configured to execute most likelihood decoding for a signal output from said first adder~~, the processor being further configured to detect an error, at a preset unit time, between a signal output from said first adder and a target signal~~, wherein

said quadratic section includes a plurality of multiplication [[unit]] units configured to multiply a first input signal and a second input signal together, one of said plurality of multiplication units being configured to employ a signal not delayed from said first input signal, as said second input signal, a remaining one of said plurality of multiplication units

being configured to employ a signal delayed a preset time from said first input signal, as said second input signal,

the one of said plurality of multiplication [[unit]] units including,

one or more series-connected delaying units configured to delay signals output from the one of said plurality of multiplication [[unit]] units each by [[the]] a preset unit time,

a multiplier configured to multiply a signal output from the one of said plurality of multiplication [[unit]] units and a signal output from each of said one or more series-connected delaying units, each with a preset coefficient, ~~said multiplier being further configured to update each preset coefficient every preset unit time based on an error detected by said processor,~~ and

a second adder configured to sum outputs of said multiplier together,

wherein a step gain parameter for updating each preset coefficient of a multiplier of the remaining one of said plurality of multiplication units is twice a step gain parameter for updating each preset coefficient of the multiplier of the one of said plurality of multiplication units.

6. (Canceled)

7. (Currently Amended) The signal decoding apparatus according to claim 5, wherein said ~~quadratic section~~ plurality of multiplication units includes n of said multiplication units, n being an integer not less than 1, a kth one of said plurality of multiplication units, k being an integer such that $1 \leq k \leq n$, being configured to employ a signal corresponding to said first input signal delayed by (k−1) times of said preset unit time, as said second input signal.

8. (Canceled)

9. (Currently Amended) A signal decoding method employing a second-order Volterra filter in equalizing and decoding an input signal, the signal decoding method comprising:

performing a processing equivalent to a linear term of said second-order Volterra filter and linearly equalizing said input signal;

performing a processing equivalent to a quadratic term of said second-order Volterra filter and non-linearly equalizing said input signal;

summing a signal output from said performing the processing equivalent to the linear term and a signal output from said performing the processing equivalent to the quadratic term together; and

most likelihood decoding a signal output from said summing~~; and detecting an error, at a unit time, between a signal output from said summing and a target signal~~, wherein

said performing the processing equivalent to the quadratic term includes,

multiplying a first input signal with a ~~second input~~ signal not delayed from said first input signal to produce a first product signal;

multiplying the first input signal with a signal delayed a preset time from said first input signal to produce a second product signal;

delaying the first product signal, by one or more series-connected delay units, each by [[the]] a unit time;

multiplying the first product signal and a signal output from each of said one or more series-connected delay units, each with a preset coefficient to produce a plurality of addend signals;

multiplying the second product signal with a preset coefficient to produce an addend signal;

~~updating each preset coefficient every unit time based on the error,~~ and

summing the addend signal and the plurality of addend signals together, wherein a step gain parameter for updating the preset coefficient for multiplying the second product signal is twice a step gain parameter for updating each preset coefficient for multiplying the first product signal and the signal output from each of said one or more series-connected delay units.

10. (Currently Amended) [[The]] A signal processing apparatus, comprising: ~~according to claim 1,~~

a second-order Volterra filter configured to equalize an input signal, wherein,

a quadratic section of said second-order Volterra filter configured to implement a quadratic term of said second-order Volterra filter includes a plurality of multiplication units configured to multiply a first input signal with a second input signal to produce a product signal, one of said plurality of multiplication units being configured to employ a signal not delayed from said first input signal, as said second input signal, a remaining one of said plurality of multiplication units being configured to employ a signal delayed a preset time from said first input signal, as said second input signal,

the one of said plurality of multiplication units including,

one or more delay units connected in series with one another and configured to delay a signal output from the one of said plurality of multiplication units, each by a unit time,

a multiplier configured to multiply the signal output from the one of said plurality of multiplication units and a signal output from each of said one or more delay units, each with a preset coefficient, and

an adder configured to sum outputs of said multiplier together,

the remaining one of said plurality of multiplication units including, ~~wherein said multiplication unit further includes~~

a shifter configured to left-shift the product signal to produce the signal output from the remaining one of said plurality of multiplication [[unit]] units, and

a multiplier configured to multiply the signal output from the remaining one of said plurality of multiplication units with a preset coefficient.

11. (Currently Amended) [[The]] A signal processing apparatus, comprising: ~~according to claim 2,~~

a second-order Volterra filter configured to equalize an input signal, wherein

a quadratic section of said second-order Volterra filter configured to implement a quadratic term of said second-order Volterra filter includes,

a plurality of multiplication units configured to multiply a first input signal with a second input signal to produce a product signal, one of said plurality of multiplication units being configured to employ a signal not delayed from said first input signal, as said second input signal, the remaining ones of said plurality of multiplication units each being configured to employ a signal delayed a preset time from said first input signal, as said second input signal,

the one of said plurality of multiplication units and one of the remaining ones of said plurality of multiplication units each including,

one or more delay units connected in series with one another and configured to delay a signal output from a respective of the one of said plurality of multiplication units and the one of the remaining ones of said plurality of multiplication units, each by a unit time,

a multiplier configured to multiply the signal output from the respective of the one of said plurality of multiplication units and the one of the remaining ones of said plurality of multiplication units, and a signal output from each of said one or more delay units, each with a preset coefficient, and

an adder configured to sum outputs of said multiplier together;

~~wherein said multiplication unit further includes,~~

a first adding unit configured to add an output from ~~a respective~~ the adder of ~~each~~ the one of the remaining ones of said plurality of multiplication units ~~together~~ with an output from another of the remaining ones of said plurality of multiplication units to produce a summed signal;

a shifter configured to left-shift the summed signal to produce a shifted signal; and

a second adding unit configured to add the shifted signal and an output from the adder of the one of said plurality of multiplication units.

12. (Canceled)

13. (New) The signal decoding apparatus according to claim 5, wherein the processor is further configured to detect an error between a signal at each discrete time output from said first adder and a target signal, said multiplier updating a preset coefficient every discrete time based on an error detected by said processor.